NLSF3T125

Quad Bus Buffer

with 3−State Control Inputs

The NLSF3T125 is a high speed CMOS quad bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The NLSF3T125 requires the 3−state control input ($\overline{OE}$) to be set High to place the output into the high impedance state.

The T125 inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The NLSF3T125 input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when V_{CC} = 0 V. These input and output structures help prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

- High Speed: t_{PD} = 3.8 ns (Typ) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 4.0 μA (Max) at T_A = 25°C
- TTL−Compatible Inputs: V_{IL} = 0.8 V; V_{IH} = 2.0 V
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model; > 2000 V, Machine Model; > 200 V
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- Pb−Free Package is Available*

FUNCTION TABLE

NLSF3T125		
Inputs		Output
A	$\overline{OE}$	Y
H	L	H
L	L	L
X	H	Z

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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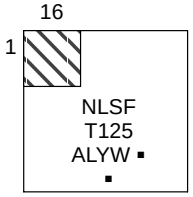
QFN−16
CASE 485G

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NLSF3T125MNR2	QFN−16	3000/Tape & Reel
NLSF3T125MNR2G	QFN−16 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Active−Low Output Enables

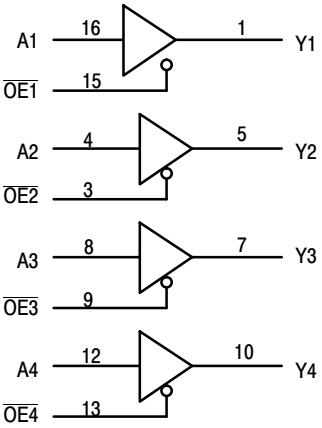


Figure 1. Logic Diagram

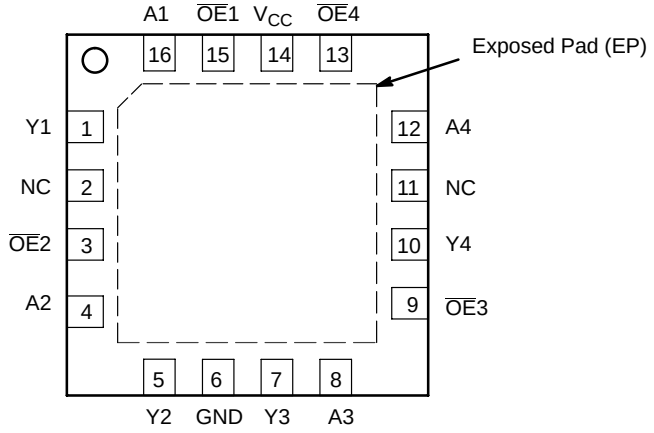


Figure 2. QFN − 16 Pinout (Top View)

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
DC Input Voltage	V_{in}	– 0.5 to + 7.0	V
DC Output Voltage Output in 3−State High or Low State	V_{out}	– 0.5 to + 7.0 – 0.5 to V_{CC} + 0.5	V
Input Diode Current	I_{IK}	− 20	mA
Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	± 20	mA
DC Output Current, per Pin	I_{out}	± 25	mA
DC Supply Current, V_{CC} and GND Pins	I_{CC}	± 75	mA
Power Dissipation in Still Air QFN Packages	P_D	500	mW
Storage Temperature	T_{stg}	– 65 to + 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	2.0	5.5	V
DC Input Voltage		V_{in}	0	5.5	V
DC Output Voltage	Output in 3−State High or Low State	V_{out}	0 0	5.5 V_{CC}	V
Operating Temperature		T_A	− 40	+ 85	°C
Input Rise and Fall Time	V_{CC} = 5.0 V ±0.5 V	t_r, t_f	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions	Symbol	V_{CC} (V)	T_A = 25°C			$T_A \le$ 85°C		$T_A \le$ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
Minimum High−Level Input Voltage	2.3 V ± 0.3 V 3.3 V ± 0.3 V 5.0 V ± 0.5 V	V_{IH}		0.5 V_{CC} 0.4 V_{CC} 0.44 V_{CC}			0.5 V_{CC} 0.4 V_{CC} 0.44 V_{CC}		0.5 V_{CC} 0.4 V_{CC} 0.44 V_{CC}		V
Maximum Low−Level Input Voltage	2.3 V ± 0.3 V 3.3 V ± 0.3 V 5.0 V ± 0.5 V	V_{IL}				0.3 V_{CC} 0.18 V_{CC} 0.18 V_{CC}		0.3 V_{CC} 0.18 V_{CC} 0.18 V_{CC}		0.3 V_{CC} 0.18 V_{CC} 0.18 V_{CC}	V
Minimum High−Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{OL} @ I_{OL}, 50 mA V_{IN} = V_{IH} or V_{IL} I_{OH} = − 50 μA	V_{OH}	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
	V_{IN} = V_{IH} or V_{IL} I_{OH} = − 2.0 mA I_{OH} = − 4.0 mA I_{OH} = − 8.0 mA		2.0 3.0 4.5	1.82 2.58 3.94			1.72 2.48 3.80		1.60 2.34 3.66		
Maximum Low−Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{OL} @ I_{OL}, 50 mA V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA	V_{OL}	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
	V_{IN} = V_{IH} or V_{IL} I_{OL} = 2.0 mA I_{OL} = 4.0 mA I_{OL} = 8.0 mA		2.0 3.0 4.5			0.36 0.36 0.36		0.44 0.44 0.44		0.52 0.52 0.52	
Maximum Input Leakage Current	V_{IN} = 5.5 V or GND	I_{IN}	0 to 5.5			± 0.1		± 1.0		± 1.0	μA
Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	I_{CC}	5.5			2.0		20		40	μA
Quiescent Supply Current	Input: V_{IN} = 3.4 V	I_{CCT}	5.5			1.35		1.50		1.65	mA
Maximum 3−State Leakage Current	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	I_{OZ}	5.5			±0.25		±2.5		±2.5	μA
Output Leakage Current	V_{OUT} = 5.5 V	I_{OPD}	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Parameter	Test Conditions	Symbol	$T_A = 25°C$			$T_A = \leq 85°C$		$T_A \leq 125°C$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
Maximum Propagation Delay, A to Y	$V_{CC} = 2.3 \pm 0.3$ V $C_L = 15$ pF	t_{PLH}, t_{PHL}	1.0	14.5	16.9	1.0	18.1	1.0	19.2	ns
	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $C_L = 50$ pF		1.0 1.0	5.6 8.1	8.0 11.5	1.0 1.0	9.5 13.0	1.0 1.0	12.0 16.0	ns
	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF		1.0 1.0	3.8 5.3	5.5 7.5	1.0 1.0	6.5 8.5	1.0 1.0	8.5 10.5	
Maximum Output Enable TIme, $\overline{OE}$ to Y	$V_{CC} = 2.3 \pm 0.3$ V $C_L = 15$ pF	t_{PZL}, t_{PZH}	1.0	14.8	16.2	1.0	17.4	1.0	19.3	ns
	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $R_L = 1.0$ kΩ $C_L = 50$ pF		1.0 1.0	5.4 7.9	8.0 11.5	1.0 1.0	9.5 13.0	1.0 1.0	11.5 15.0	ns
	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $R_L = 1.0$ kΩ $C_L = 50$ pF		1.0 1.0	3.6 5.1	5.1 7.1	1.0 1.0	6.0 8.0	1.0 1.0	7.5 9.5	
Maximum Output Disable Time, $\overline{OE}$ to Y	$V_{CC} = 2.3 \pm 0.3$ V $C_L = 15$ pF	t_{PLZ}, t_{PHZ}	1.0	15.4	18.0	1.0	19.8	1.0	22.0	ns
	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 50$ pF $R_L = 1.0$ kΩ		1.0	9.5	13.2	1.0	15.0	1.0	18.0	ns
	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF $R_L = 1.0$ kΩ		1.0	6.1	8.8	1.0	10.0	1.0	12.0	ns
Output−to−Output Skew	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 50$ pF (Note 1)	t_{OSLH}, t_{OSHL}			1.5		1.5		2.0	ns
	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF (Note 1)				1.0		1.0		1.5	
Maximum Input Capacitance		C_{in}		4	10		10		10	pF
Maximum Three−State Output Capacitance (Output in High Impedance State)		C_{out}		6						pF
			Typical @ 25°C, $V_{CC} = 5.0$V							
Power Dissipation Capacitance (Note 2)		C_{PD}	15							pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per buffer). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

Characteristic	Symbol	$T_A = 25°C$		Unit
		Typ	Max	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	0.3	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	− 0.3	− 0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.5	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		1.5	V

SWITCHING WAVEFORMS

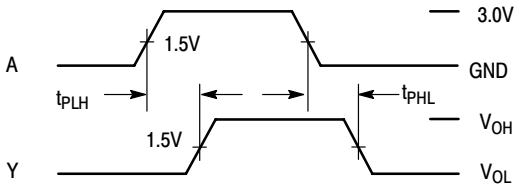


Figure 3.

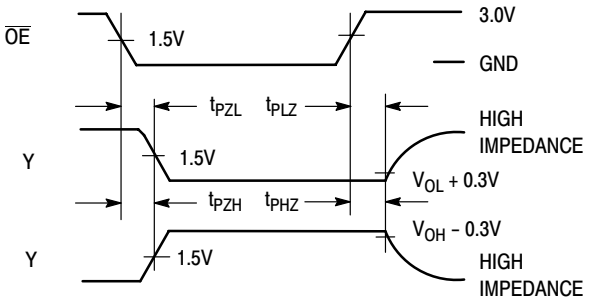
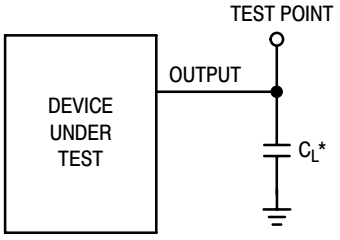
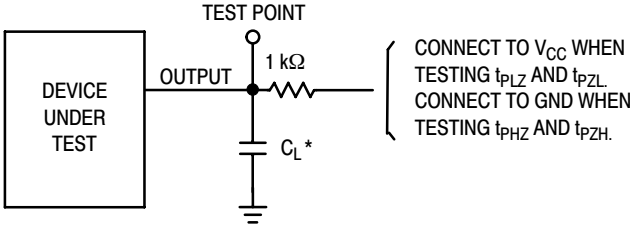


Figure 4.



*Includes all probe and jig capacitance

Figure 5. Test Circuit

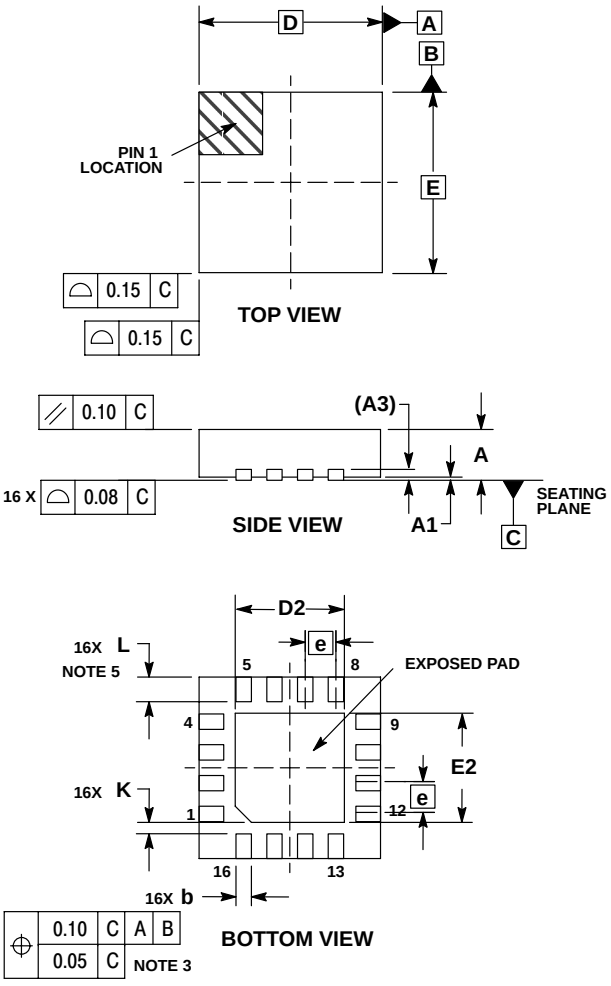


*Includes all probe and jig capacitance

Figure 6. Test Circuit

PACKAGE DIMENSIONS

16 PIN QFN
CASE 485G−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.18 TYP	
L	0.30	0.50

PUBLICATION ORDERING INFORMATION

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